AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An integrated circuit comprising:

a data processing circuit ~~operable~~ configured to perform data processing operations;

a processor, responsive to program instructions, ~~operable to perform~~ for performing non-diagnostic data processing operations under program instruction control; and

a diagnostic circuit coupled to said data processing circuit and operable to capture diagnostic data relating to said data processing circuit;

wherein said processor is also coupled to said diagnostic circuit and is ~~operable~~ responsive to program instructions to perform diagnostic data processing operations including accessing ~~access~~ said diagnostic data relating to said data processing circuit independently of said data processing circuit.

2. (Currently Amended) An integrated circuit as claimed in claim 1, wherein said diagnostic circuit is ~~operable~~ configured upon detecting predetermined conditions to halt data processing by said data processing circuit to provide halting mode debug.

3. (Currently Amended) An integrated circuit as claimed in claim 1, wherein said diagnostic circuit is ~~operable~~ configured to capture diagnostic code profiling data relating to program instructions being executed by said data processing circuit whilst said data processing circuit continues to execute program instructions.

4. (Currently Amended) An integrated circuit as claimed in claim 1, wherein said diganostic circuit is ~~operable~~ configured upon detecting predetermined conditions to trigger said data processing circuit to execute an exception handling program to provide monitor mode debug.

5. (Currently Amended) An integrated circuit as claimed in claim 1, wherein said processor is ~~operable~~ configured to control output of said diagnostic data relating to said data processing circuit from said integrated circuit.

6. (Currently Amended) An integrated circuit as claimed in claim 1, wherein said processor is ~~operable~~ configured to control said diagnostic circuit to perform diagnostic operations upon said data processing circuit.

7. (Currently Amended) An integrated circuit as claimed in claim 1, wherein said data processing circuit and said processor are configured to communicate during non-diagnostic operation via a system bus.

8. (Currently Amended) An integrated circuit as claimed in claim 1, wherein said data processing circuit and said processor are configured to communicate during diagnostic operation via a diagnostic bus.

9. (Currently Amended) An integrated circuit as claimed in claim 7, comprising a bus bridge between said system bus and a diagnostic bus, said data processing circuit and said processor are configured to communicate ~~communicating~~ during diagnostic operation via said system bus, said bus bridge and said diagnostic bus.

10. (Currently Amended) An integrated circuit as claimed in claim 1, wherein said diagnostic circuit is ~~operable~~ configured to store said diagnostic data relating to said data processing circuit within memory mapped storage locations accessible by said processor.

11. (Currently Amended) An integrated circuit as claimed in claim 1, comprising:
a processor diagnostic circuit coupled to said processor and ~~operable~~ configured upon detecting predetermined conditions to halt program instruction execution by said processor and capture diagnostic data relating to said processor; wherein

said data processing circuit is also coupled to said processor diagnostic circuit and is ~~operable~~ configured to access said diagnostic data said relating to said processor.

12. (Currently Amended) An integrated circuit as claimed in claim 1, comprising a peripheral device communication circuit ~~operable~~ configured during non-diagnostic operation of said integrated circuit to provide data communication with an external operational device coupled to said integrated circuit, said peripheral device communication circuit being ~~used~~ useable by said processor during diagnostic operation to communicate at least one of said diagnostic data relating to said data processing circuit, diagnostic operations and pre-processed diagnostic data with an external diagnostic device.

13. (Original) An integrated circuit as claimed in claim 9, wherein said bus bridge is coupled via a diagnostic interface to an external diagnostic device.

14. (Currently Amended) An integrated circuit as claimed in claim 1, wherein said data processing circuit is a further processor ~~operable~~ configured to perform data processing operations under program instruction control.

15. (Currently Amended) A method of obtaining diagnostic data for an integrated circuit comprising the steps of:

performing data processing operations with a data processing circuit within said integrated circuit;

performing non-diagnostic data processing operations under program instruction control with a processor within said integrated circuit;

capturing with a diagnostic circuit coupled to said data processing circuit and within said integrated circuit diagnostic data relating to said data processing circuit; and

performing diagnostic data processing operations with said processor under program instruction control including accessing said diagnostic data said relating to said data processing circuit with said processor and independently of said data processing circuit.

16. (Currently Amended) A method as claimed in claim 15, wherein said diagnostic circuit, ~~is operable~~ upon detecting predetermined conditions, ~~to halt~~ halts data processing by said data processing circuit to provide halting mode debug.

17. (Currently Amended) A method as claimed in claim 15, wherein said diagnostic circuit ~~is operable to capture~~ captures diagnostic code profiling data relating to program instructions being executed by said data processing circuit whilst said data processing circuit continues to execute program instructions.

18. (Currently Amended) A method as claimed in claim 15, wherein said diagnostic circuit, ~~is operable~~ upon detecting predetermined conditions, ~~to~~ triggers said data processing circuit to execute an exception handling program to provide monitor mode debug.

19. (Currently Amended) A method as claimed in claim 15, wherein said processor ~~is operable to control~~ controls output of said diagnostic data relating to said data processing circuit from said integrated circuit.

20. (Currently Amended) A method as claimed in claim 15, wherein said processor ~~is operable to control~~ controls said diagnostic circuit to perform diagnostic operations upon said data processing circuit.

21. (Original) A method as claimed in claim 15, wherein said data processing circuit and said processor communicate during non-diagnostic operation via a system bus.

22. (Original) A method as claimed in claim 15, wherein said data processing circuit and said processor communicate during diagnostic operation via a diagnostic bus.

23. (Original) A method as claimed in claim 21, wherein said data processing circuit and said processor communicate during diagnostic operation via said system bus, a bus bridge and a diagnostic bus.

24. (Currently Amended) A method as claimed in claim 15, wherein said diagnostic circuit ~~is operable to store~~ stores said diagnostic data relating to said data processing circuit within memory mapped storage locations accessible by said processor.

25. (Currently Amended) A method as claimed in claim 15, wherein:
a processor diagnostic circuit is coupled to said processor ~~is operable~~ and upon detecting predetermined conditions ~~to halt~~ halts program instruction execution by said processor and to capture diagnostic data relating to said processor; and
said data processing circuit is also coupled to said processor diagnostic circuit and ~~is operable to access~~ accesses said diagnostic data said relating to said processor.

26. (Currently Amended) A method as claimed in claim 15, wherein a peripheral device communication circuit, ~~is operable~~ during non-diagnostic operation of said integrated circuit, ~~to provide~~ provides data communication with an external operational device coupled to said integrated circuit, said peripheral device communication circuit being used by said processor during diagnostic operation to communicate at least one of said diagnostic data relating to said data processing circuit, diagnostic operations and pre-processed diagnostic data with an external diagnostic device.

27. (Currently Amended) A method as claimed in claim 23, wherein said bus bridge is coupled via a diagnostic interface to an external diagnostic device.

28. (Currently Amended) A method as claimed in claim 15, wherein said data processing circuit is a further processor ~~operable to perform~~ performing data processing operations under program instruction control.

29. (Currently Amended) A computer program product embodied on a computer-readable medium having a computer program operable to control a processor to obtain diagnostic data for an integrated circuit in accordance with the method of claim 15.